A Flexible Heterogeneous Video Processor System for Television Applications.

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ABSTRACT

A new video processing architecture for TV applications is presented, featuring a flexible heterogeneous multi-processor architecture executing video tasks in parallel and independently. The signal flow graph and the processors are programmable, enabling an optimal picture quality for different TV display modes. The concept is verified by an experimental chip design.

INTRODUCTION

The development for high-quality television and the strong emerge of Internet for information retrieval and commercial applications, lead to the design of a new TV set with much more flexibility and openness to new TV features than was usual in the past. A key feature of this set is that two signals (or more) can be monitored on a TV display together with graphical information. The design of such a flexible TV set differs significantly from that of conventional designs. Up till now, a secondary video signal on the display is mostly realized with additional dedicated hardware. This hardware is minimized for limiting costs, thereby sacrificing the picture quality. In the new design, it is pursued that additional signals are shown with equal priority and picture quality. In order to fulfill this requirement, an equal amount of signal processing capacity should be available for the individual video channels. It is our aim to realize this without doubling or tripling the processing hardware and –not in the least– the corresponding memory.

ARCHITECTURE CONCEPT

The above-mentioned requirements have been solved by sharing the hardware and memory for similar signal processing and by enabling a higher clock frequency. Bearing this strategy in mind, a new chip set for high-end TV applications is designed. The key features of the chip set are that:

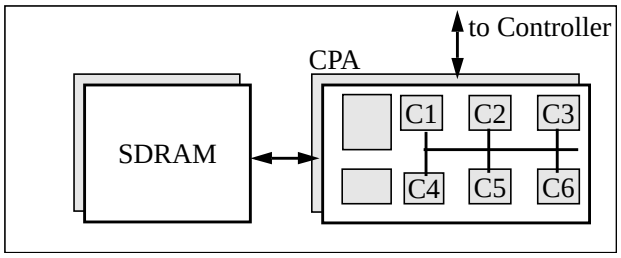

Figure 1: Hardware architecture of the CPA IC.

- comparable TV functions are mapped on the *same* hardware processing unit ( );
- large field memories and other similar storage functions are shared in the *same background memory*;
- the processing hardware runs on a *multiple* of the intrinsical video clock rate to enable sufficient parallelism;
- a communication structure with sufficient parallelism provides simultaneous transfer of multiple data streams.

This novel concept has been used to implement a set of enhancement and signal mixing functions of a high-end TV receiver. It is interesting to implement this part of the TV receiver with this new architecture, because in the enhancement part, sharing of memory and signal processing hardware would be most beneficial. The TV signal processing functions considered are a.o.

– horizontal and vertical scaling of video to any display format (see e.g. [2]);
– adaptive noise reduction;
– sharpness improvement [1] for both luminance and colour;
– field-rate conversion.

Figure 1 shows that the system is based on a number of processing units, which can performe a video function for a few signals simultaneously. The way the processing units are connected is programmable, so that the sequential order of TV processing functions is flexible. Given the diverse nature of video

functions in a TV, the complexity and latency of each function can be very different. Each coprocessor is an autonomous unit, independent of all other processors in the system and it is optimized for executing its own functionality. The data communication between processor is defined by simple *data-driven* communication rules. These rules are according to Kahn's language for parallel programming [4], in which one axiom is that data is processed only when video data is received and available at the input. It has been shown that large multi-processor systems build upon such processing units can execute programmable signal flow graphs (dynamic data flow). This is enabled by using synchronous (deterministic) processing functions and run-time scheduling [5].

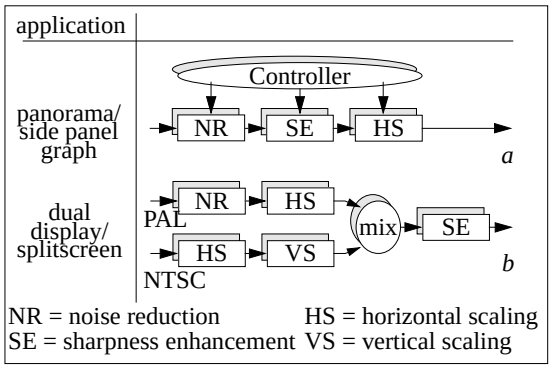

Figure 2: Same coprocessors used in different configurations and settings (50 Hz system).

FLEXIBILITY AND PROGRAMMABILITY

The system allows two forms of programmability. Firstly, each function has been made programmable in performance by using *parameterizable* signal processing functions. The parameter setting of functions can be optimized depending on other TV functions in the flow graph, e.g. more sharpness enhancement is applied when zooming is used. This property allows optimal performance for the total chain of signal processing functions.

The second form of programmability is that a function can be re-used for more than one signal stream simultaneously, for different applications and with individual parameter settings. This property enables a large variety of features. For example, Fig. 2 shows that the horizontal scaler is used consecutively for geometric conversion (widescreen), compression and pixel-rate adaptation. The result is that the aforementioned display functions can be used in an arbitrary order and at different positions in the signal flow-graph in the TV processor (see Fig. 2), a new phenomenon in a TV receiver.

HARDWARE

The underlying hardware architecture of the system consists of an array of coprocessors (CPA, see Fig. 1) with flexible interconnections and running on a clock frequency of 64 MHz. This allows up to four TV signals of 16 MHz clock rate to be processed in parallel.

The interconnections are implemented by a fully programmable switch matrix, which supports any connection between coprocessors to transfer video streams. This matrix concept was adopted earlier for programmable video processing applications [3]. As a result, virtually any type of signal flow-graph can be programmed into the IC, which makes the application area highly versatile. Furthermore, it can be concluded that this coprocessor-array architecture is well scalable and extensible to the future by adding new processing units. As a bonus, in any new configuration, the picture quality setting and the order of signal processing tasks can be re-optimized for the new set of coprocessors and the corresponding applications.

An experimental IC with the specification from Table 1 is being designed and will become available in the second half of 1998.

Table 1. Key parameters of experimental CPA IC.

coprocessors	6 types
input/output proc.	3 / 2
Hor. resolution	$\leq$ 848 samples
Ver. resolution	$\leq$ 600 lines
Clock frequency	64 MHz
External memory	96 MHz SDRAM
memory bus bandw.	$\leq$ 384 MByte/s

References

[1] E.G.T. Jaspers and P.H.N. de With, "A Generic 2D Sharpness Enhancement Algorithm for Luminance Signals", Sixth Conf. Image Proc. & its Applic. IPA97, Dublin 1997, Vol. 1, pp. 269–273, July 1997.

[2] J.G.W.M. Janssen, J. Stessen and P.H.N. de With, "An Advanced Sampling Rate Conversion technique for Video and Graphics Signals", Sixth Conf. Image Proc. and its Applic. IPA97, Dublin 1997, Vol. 2, pp. 771–775, July 1997.

[3] H.J.M. Veendrick *et.al*, "A 1.5 Gips Video Signal Processor (VSP)", Proc. CICC, 6.2, San Diego CA, May 1994.

[4] G. Kahn, "The Semantics of a Simple Langue for Parallel Programming", Information Processing 74 (Proc. of IFIP congress 1974), pp. 471-475, August 1974.

[5] J.T. Buck and E.A. Lee, " Scheduling Dynamic Dataflow Graphs with Bounded Memory using the Token Model", Proc. of ICASSP '93, Vol 1, pp. 429-432, April 1993.